

AC7006F Datasheet

Zhuhai Jieli Technology Co.,LTD

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AC7006F Features

CPU

- 32bit Dual-Issue DSP
- Up to 160MHz programmable processor
- With IEEE754 Single precision FPU
- With cordic accelerate engine
- Advanced debug with 8 hardware breakpoints/watchpoints
- Advanced system exception capture unit

Interrupt

- Support for up to 64 interrupts with 8 priority level
- NMI supported
- SWI supported, with configurable priority
- Low power wake up by polling pending 12 IO interrupts for low power wake up

DSP Audio Processing

- SBC, AAC Audio decodes supported for BT audio
- mSBC voice codec supported for BT phone
- Supports MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Single/Dual MIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- 20-band EQ configuration for voice Effects

Audio Codec

- Two channels 24-bit DAC, SNR \geq 102dB
- Two channels 24-bit ADC, SNR \geq 95dB
- DAC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz/64kHz/88.2kHz/96kHz are supported
- ADC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz are supported

- Two analog MIC amplifier, build-in MIC bias generator
- Supports Four PDM digital MIC inputs
- Two channels analog AUX, supports stereo
- Supports cap-less, single-ended, and Two differential mode at the DAC path
- Supports 16ohm and 32ohm Speaker loading

ANC

- ANC processing engine up to 750 kHz sample rate
- 7.5 μ s analog to analog latency
- Supports 4 digital microphone inputs, 2 differential or single-ended analog inputs for ANC
- Supports 2 channels Feed-Forward, Feed-Back, Hybrid ANC
- ANC module include 20 double precision Biquad filters for each FF/FB/ music compensation control

Bluetooth

- Compliant with Bluetooth V5.3+BR+EDR+BLE specification
- Meet class2 and class3 transmitting power requirement
- Support GFSK and DQPSK all packet types
- Provides a maximum +10dbm transmitting power
- EDR receiver with -94dBm sensitivity
- Fast AGC for enhanced dynamic range
- Supports
 - a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap\gatt\rfcomm\sdp\l2cap profile
 - a2dp 1.3.2\avctp 1.4\avdtp 1.3\ avrcp 1.6.2\hfp 1.8 \spp 1.2\rfcomm 1.1\pnp 1.3\hid 1.1.1\sdp core5.3\l2cap core 5.3

Peripherals

- One full speed USB 2.0 OTG controller
- Six multi-function 32-bit timers, support

- capture and PWM mode
- Three full-duplex basic UART, UART0, UART1 support DMA mode
- One hardware IIC interface supports host and device mode
- Three Built-in low power Cap Sense Keys
- LED controller, support 2 LED control by one IO
- 10-bit ADC for analog sampling
- External wake up/interrupt on all GPIOs
- Crossbar IO support: timer\SPI\SDC\IIC\UART\RDEC\ALINK\PLINK

PMU

- Low voltage LDO and DC-DC for internal digital and analog circuit supply
- Less 2uA current consumption in the soft-off mode

- Built-in LDO and DC-DC for the core, I/O, Bluetooth and flash
- VBAT is 2.2V to 4.4V
- IOVDD is 2.2V to 3.6V

Packages

- QFN32(4mm*4mm)

Temperature

- Operating temperature: -40°C to +85°C
- Storage temperature: -65°C to +150°C

Applications

- Bluetooth Stereo Headsets and Headphones
- Bluetooth Stereo ANC Headsets and Headphones
- Bluetooth ANC TWS Earphones

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1、 Pin Definition

1.1 Pin Assignment

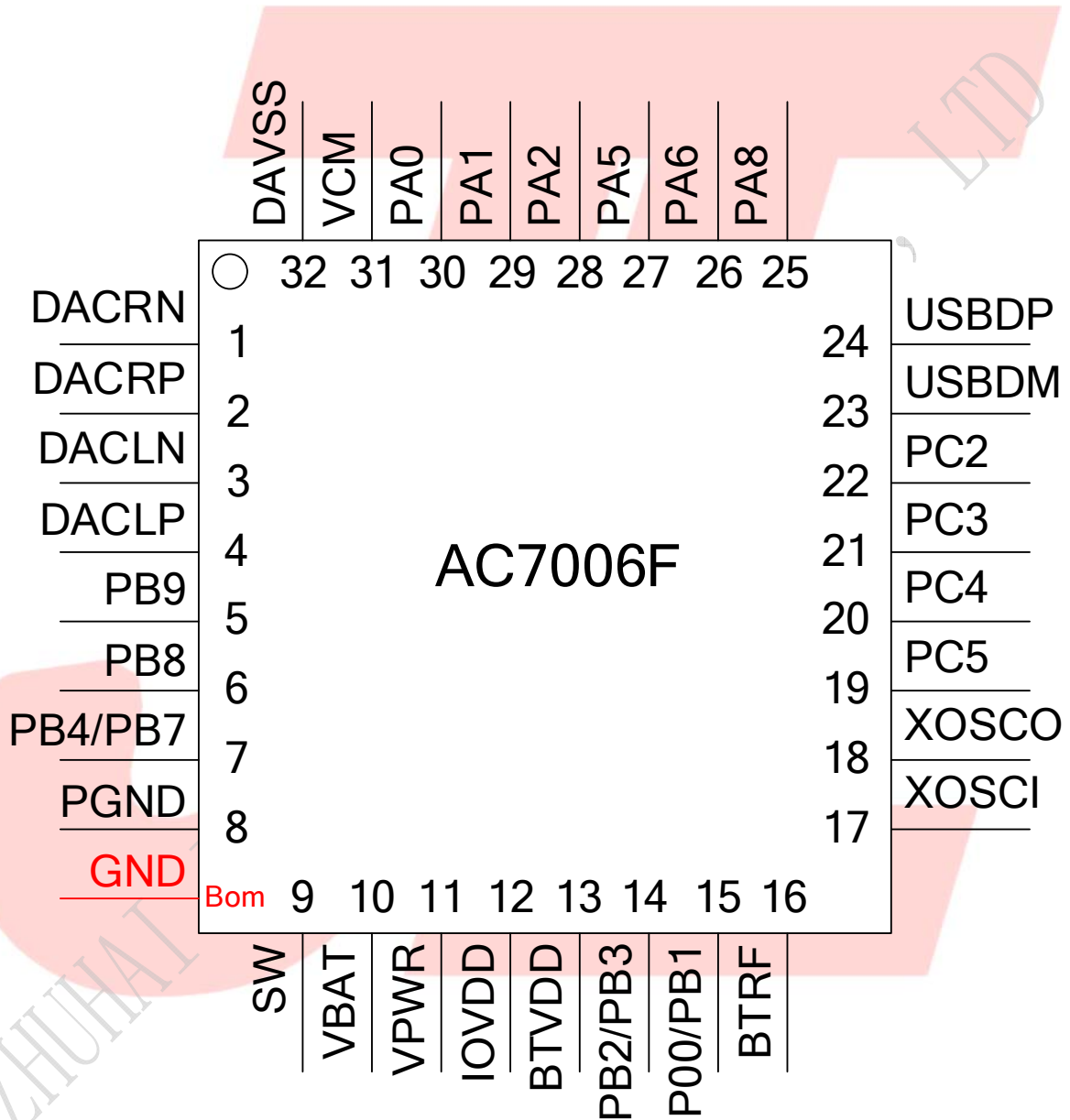


Figure 1-1 AC7006F Package Diagram

1.2 Pin Description

Table 1-1 AC7006F Pin Description

PIN NO.	Name	I/O Type	Drive (mA) 4 level	Function	Other Function
1	DACRN	O	/		Different DAC Right Negative Channel
2	DACRP	O	/		Different DAC Right Positive Channel
3	DACLN	O	/		Different DAC Left Negative Channel
4	DACL P	O	/		Different DAC Left Positive Channel
5	PB9	I/O	2.4~64	GPIO	
	SDPG	PO	/		SDPG: Supply voltage to SD Card
6	PB8	I/O	2.4~64	GPIO	MIC1: MIC1 Input Channel; MIC1_P: Different MIC1 Positive AMUX_B0: Analog Channel B0 L/R Input; UART0RXB: Uart0 Data Input(B); CAP4: Timer4 Capture;
7	PB7	I/O	2.4~64	GPIO	MIC_BIAS1: MIC1 Bias Output; MIC1_N: Different MIC1 Negative AMUX_B1: Analog Channel B1 L/R Input;; UART0TXB: Uart0 Data Output(B);
	PB4	I/O	2.4~64	GPIO	LP_TH3: Low Power Touch Channel 3 ADC8: ADC Input Channel 8; TMR2: Timer2 Clock Input; LVD:
8	PGND	P	/		DCDC Ground
9	SW	P	/		DCDC switch output, connected to inductor
10	VBAT	PI	/		Power Supply, connect to battery
11	VPWR	PI	/		Charge Power Input;
		I/O	8	GPIO	High Voltage Resistance I/O; UART0TXC: Uart0 Data Output(C); UART0RXC: Uart0 Data Input(C); PWM3: Timer3 PWM Output; CAP1: Timer1 Capture;
12	IOVDD	PO	/		IO Power 3.3v
13	BTVDD	PO	/	GPIO	BT Power
14	PB2	I/O	2.4~64	GPIO	LP_TH2: Low Power Touch Channel 2

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					ADC7: ADC Input Channel 7; CAP5: Timer5 Capture; UART2RXC: Uart2 Data Input(C); SPI2DOC: SPI2 Data Out(C);
	PB3	I/O	2.4~64	GPIO	
	EVDD	PO	/		EVDD: Supply voltage to Peripherals
15	P00	I/O	8		Test pin
	PB1	I/O	2.4~64	GPIO (pull up)	Long Press Reset; LP_TH1: Low Power Touch Channel 1 UART2TXC: Uart2 Data Output(C) ADC6: ADC Input Channel 6; SPI2CLKC: SPI2 Clk(C);
16	BTRF	/	/		BT Antenna
17	XOSCI	I	/		XOSC In
18	XOSCO	O	/		XOSC Out
19	PC5	I/O	2.4~64	GPIO	SD0CLKA: SD0 Clock(A); UART2RXD: Uart2 Data Input(D); SPI1DOB: SPI1 Data Out(B); ALNK_DAT3(B): Audio Link Data3(B); IIC_SDA_B: IIC SDA(B); ADC5: ADC Input Channel 5;
20	PC4	I/O	2.4~64	GPIO	SD0CMDA: SD0 CMD(A); UART2TXD: Uart2 Data Output(D); SPI1CLKB: SPI1 Clock(B); ALNK_DAT2(B): Audio Link Data2(B); IIC_SCL_B: IIC SCL(B); ADC4: ADC Input Channel 4; PWM4: Timer4 PWM Output;
21	PC3	I/O	2.4~64	GPIO	SD0DATA: SD0 Data(A); UART0RXD: Uart0 Data Input(D); SPI1DIB: SPI1 Data In(B); ALNK_LRCK(B): Audio Link Word Select(B); IIC_SDA_C: IIC SDA(C); TMR3: Timer3 Clock Input;
22	PC2	I/O	2.4~64	GPIO	ALNK_SCLK(B): Audio Link Serial Clock(B); IIC_SCL_C: IIC SCL(C); UART0TXD: Uart0 Data Output(D); TMR1: Timer1 Clock Input;
23	USBDM	I/O	4	USB Negative Data	UART1RXD: Uart1 Data Input(D); IIC_SDA_A: IIC SDA(A); ADC11: ADC Input Channel 11;

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					SPI2DOB: SPI2 Data Out(B); ISP_DI:
24	USBDP	I/O	4	USB Positive Data	UART1TXD: Uart1 Data Output(D); IIC_SCL_A: IIC SCL(A); ADC10: ADC Input Channel 10; SPI2CLKB: SPI2 Clock(B); ISP_CLK:
25	PA8	I/O	2.4~64	GPIO	ALNK_LRCK(A): Audio Link Word Select(A); UART2RXB: Uart1 Data Input(B); PLNK_DAT1: PLNK Data1; ADC3: ADC Input Channel 3;
26	PA6	I/O	2.4~64	GPIO	ALNK_DAT3(A): Audio Link Data3(A); UART0RXA: Uart1 Data Input(A); PLNK_DAT0: PLNK Data0; IIC_SDA_D: IIC SDA(D); ADC2: ADC Input Channel 2; CAP0: Timer0 Capture; SPI2DOA: SPI2 Data Out(A);
27	PA5	I/O	2.4~64	GPIO	ALNK_DAT2(A): Audio Link Data2(A); UART0TXA: Uart0 Data Output(A); PLNK_SCLK: PLNK Serial Clock; IIC_SCL_D: IIC SCL(D); ADC1: ADC Input Channel 1; PWM5: Timer5 PWM Output; SPI2CLKA: SPI2 Clock(A);
28	PA2	I/O	2.4~64	GPIO	ALNK_MCLK(A): ALNK Master Clock(A); MIC_BIAS0: MIC0 Bias Output; MIC0_N: Different MIC0 Negative AMUX_A1: Analog Channel A1 L/R Input; CAP3: Timer3 Capture; UART1RXC: Uart1 Data In(C); CLKOUT1:
29	PA1	I/O	2.4~64	GPIO	MIC0: MIC0 Input Channel ; MIC0_P: Different MIC0 Positive AMUX_A0: Analog Channel A0 L/R Input; PWM0: Timer0 PWM Output; UART1TXC: Uart1 Data Output(C);
30	PA0	I/O	2.4~64	GPIO	MIC Power Supply
31	VCM	P	/		DAC reference voltage
32	DAVSS	P	/		Analog Ground
/	Bom	P	/		Ground

P: Power or Ground PO:Power Output PI:Power Input I/O:Input or Output I:Input O:Output

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2、Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	4.5	V
VPWR	Charger Voltage	-0.3	6	V
V _{3.0IO}	3.0V IO Input Voltage (IOVDD)	-0.3	3.6	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	4.4	V	
VPWR	Charger supply Voltage	4.5	5.0	5.5	V	
Normal mode						
IOVDD	Voltage output	–	3.0	–	V	VBAT = 4.2V, 10mA loading
	Loading current	–	–	100	mA	IOVDD=3.0V@VBAT = 4.2V
BTVDD	Voltage output	–	1.25	–	V	IOVDD=3.0V, 10mA loading
	Loading current	–	–	60	mA	BTVDD=1.25V@IOVDD=3.0v
EVDD	Voltage output	–	1.1	–	V	BTVDD=1.25V, 1mA loading
	Loading current	–	–	5	mA	EVDD=1.1V@BTVDD=1.25v
LP mode						
IOVDD	Loading current			5	mA	IOVDD=3V@VBAT = 4.2V

2.3 Battery Charge

Table 2-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VPWR	Charge Input Voltage	4.5	5	5.5	V	–
V _{Charge}	Charge Voltage	4.15	4.2	4.25	V	VPWR > 4.5V
		4.30	4.35	4.40	V	VPWR > 4.65V

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I _{Charge}	Charge Current	20		200	mA	Charge current at fast charge mode
I _{Trickl}	Trickle Charge Current	20	45	70	mA	V _{BAT} <V _{Trickl}

2.4 IO Input/Output Electrical Logical Characteristics

Table 2-4

IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Low-Level Input Voltage	-0.3	—	0.3* IOVDD	V	IOVDD = 3.0V
V _{IH}	High-Level Input Voltage	0.7* IOVDD	—	IOVDD+0.3	V	IOVDD= 3.0V
IO output characteristics						
V _{OL}	Low-Level Output Voltage	—	—	0.33	V	IOVDD= 3.0V
V _{OH}	High-Level Output Voltage	2.7	—	—	V	IOVDD = 3.0V

2.5 Internal Resistor Characteristics

Table 2-5

Port	Drive(mA)				Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA0~PA8 PB1~PB9 PC2~PC5	2.4	8	26.4	64	10K	10K	1、PB1 default pull up 2、USBDM & USBDP default pull Down
PP0(VPWR), P00	8				10K	10K	3、PP0(VPWR), P00 are high voltage resistance to 5V
USBDP	4				1.5K	15K	4、internal pull-up/pull-down resistance accuracy ±20%
USBDM	4				180K	15K	

2.6 DAC Characteristics

Table 2-6

Parameter	Min	Typ	Max	Unit	Audio Format	Test Conditions
Frequency Response	20	—	20K	Hz	—	Differential Mode
Output Swing		0.55	0.71	V _{rms}	—	1KHz/0dB
THD+N	—	-78	—	dB	PCM	32 ohm loading
	—	-69.4	—	dB	SBC	With A-Weighted

S/N	-	100	102	dB	PCM	Filter
	-	99.5	-	dB	SBC	
Crosstalk	-	-110.0	-	dB	-	
Dynamic Range	-	100.2	-	dB	PCM	Differential Mode 1KHz/-60dB 32 ohm loading With A-Weighted Filter
	-	100	-	dB	SBC	
Noise Floor	-	6.0	-	uVrms	-	A-Weighted Filter
DAC Output Power	-	9.5	16.0	mW	-	Differential Mode 32ohm loading

2.7 ADC Characteristics

Table 2-7

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range		95		dB	Fsample=44.1kHz Fin=1KHz 2mVpp Input
SNR	-	95	-	dB	Fsample=44.1kHz Fin=1KHz 2Vpp Input
THD+N	-	-72	-	dB	
Crosstalk	-	-80	-	dB	

2.8 BT Characteristics

2.8.1 Transmitter

Basic Data Rate

Table 2-8

Parameter	Min	Typ	Max	Unit	Test Conditions
RF Transmit Power		8	10	dBm	25°C, Power Supply
RF Power Control Range		18.2		dB	
20dB Bandwidth		950		KHz	
Adjacent Channel	+2MHz	-40		dBm	VBAT=3.7V 2441MHz 2 Layer Board
	-2MHz	-38		dBm	
Transmit Power	+3MHz	-44		dBm	
	-3MHz	-35		dBm	

Enhanced Data Rate Table 2-9

Parameter		Min	Typ	Max	Unit	Test Conditions
Relative Power			-1.2		dB	25°C, Power Supply VBAT=3.7V 2441MHz 2 Layer Board
$\pi/4$ DQPSK	DEVM RMS	6	11.4		%	
	DEVM 99%	10	19.7		%	
	DEVM Peak	15	24.8		%	
Modulation Accuracy	+2MHz		-40		dBm	
Adjacent Channel	-2MHz		-38		dBm	
Transmit Power	+3MHz		-44		dBm	
	-3MHz		-35		dBm	

2.8.2 Receiver

Basic Data Rate Table 2-10

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-92		dBm	25°C, Power Supply VBAT=3.7V 2441MHz DH5 2 Layer Board
Co-channel Interference Rejection			-10		dB	
Adjacent Channel	+1MHz		+4		dB	
	-1MHz		+2		dB	
	+2MHz		+38		dB	
Interference Rejection	-2MHz		+38		dB	
	+3MHz		>+40		dB	
	-3MHz		+34		dB	

Enhanced Data Rate Table 2-11

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-94		dBm	25°C, Power Supply VBAT=3.7V 2441MHz 2DH5 2 Layer Board
Co-channel Interference Rejection			-11		dB	
Adjacent Channel	+1MHz		+4		dB	
	-1MHz		+2		dB	
	+2MHz		+38		dB	
Interference Rejection	-2MHz		+38		dB	
	+3MHz		>+40		dB	
	-3MHz		+34		dB	

3、 Package Information

3.1 QFN32_4.0x4.0

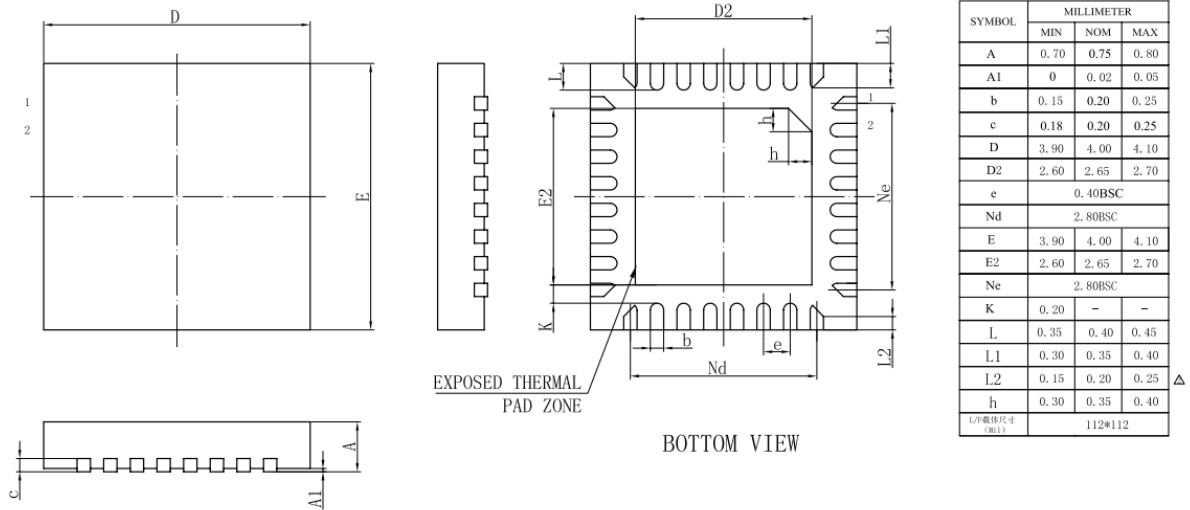
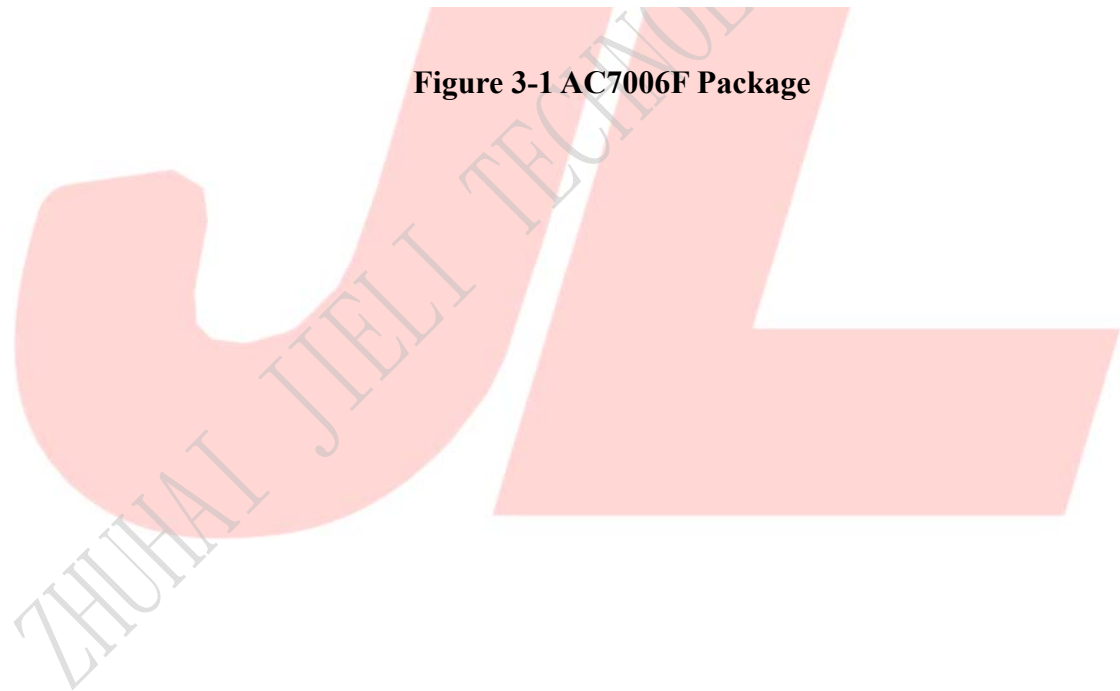


Figure 3-1 AC7006F Package



4、Revision History

Date	Revision	Description
2021.05.13	V1.0	Initial Release
2021.05.27	V1.1	Update Electrical Characteristics
2021.08.03	V1.2	Update Bluetooth Vision and profile, Update Audio and Bluetooth Characteristics

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