

AC7023E Datasheet

Zhuhai Jieli Technology Co.,LTD

Version: 1.3

Date: 2024.09.29

AC7023E Features

CPU

- 32-bit DSP
- with IEEE754 Single precision FPU
- Up to 160MHz programmable processor
- 64Vectored interrupts
- 8 Levels interrupt priority

Clocks

- 24 MHz crystal oscillator

DSP Audio Processing

- SBC, AAC Audio decodes supported for BT audio
- mSBC voice codec supported for BT phone
- Packet Loss Concealment (PLC) for voice processing
- Single MIC Environmental Noise Cancellation (ENC)
- Single-band DRC limiter
- Multi-band EQ configuration for voice Effects

Audio Codec

- Two channels 24-bit DAC,SNR maximum 98dB
- One channels 16-bit ADC,SNR maximum 85dB
- Audio DAC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz are supported
- Audio ADC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz are supported
- One channels analog audio inputs
- Audio DAC supports differential cap-less mode or single-ended mode or vcmo-sterero mode
- Direct drive 16ohm/32ohm Speaker loading

Bluetooth

- Compliant with Bluetooth

V5.4+BR+EDR+BLE specification
(QDID: 223418)

- Meet class2 and class3 transmitting power requirement
- Maximum +8dbm transmitting power
- EDR receiver with minimum -94dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap\gatt\rfcomm\sdpl2cap profile
- A2DP 1.4\AVCTP 1.4\AVDTP 1.3\AVRCP 1.6.2\HFP 1.8\SPP 1.2\RFCOMM 1.2\PNP 1.3\HID 1.1.1\SDP core5.4\L2CAP core 5.4

Peripherals

- full speed USB OTG controller
- multi-function 32-bit timers, support capture and PWM mode
- Uart interface support DMA
- I2C Master/Slave interface
- Low power CapSense
- 10-bit ADC for analog sampling
- Individually programmable and multiplexed GPIO pins
- external interrupt/wake-up source(low power available,can be multiplexed to any I/O)

PMU

- Built-in lithium battery charging manager,up to 200mA charging current
- Built-in LDO and Buck DC-DC converter
- Soft-off mode current
- Build-in LP_Touch off: $\leq 3\mu\text{A}(\text{AC702N_FLASH_SDK_vx.x.x})$
 $\leq 7\mu\text{A}(\text{AC702N_release_vx.x.x})$
- Build-in LP_Touch on: $\leq 13\mu\text{A}$
- VPWR range : 4.5V to 5.5V
- VBAT range : 2.7V to 4.5V
- IOVDD range : 2.0V to 3.4V

Packages

- QFN20(3mm*3mm)

Temperature

- Operating temperature: -40°C to +85°C
- Storage temperature: -65°C to +150°C

Applications

- Bluetooth Stereo Headset and Headphone
- Bluetooth Lightning Earphone



1 Block Diagram

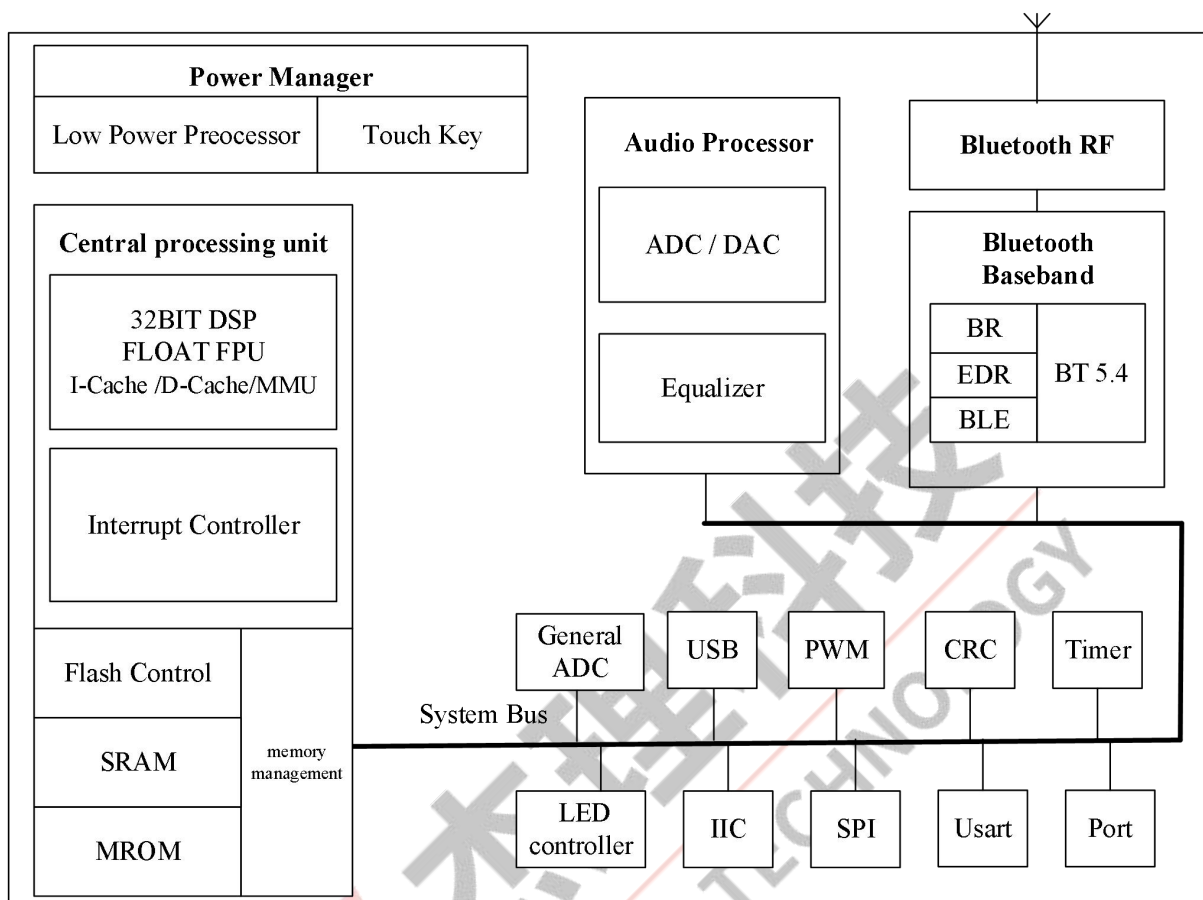


Figure 1-1 AC7023E Block Diagram

2 Pin Definition

2.1 Pin Assignment

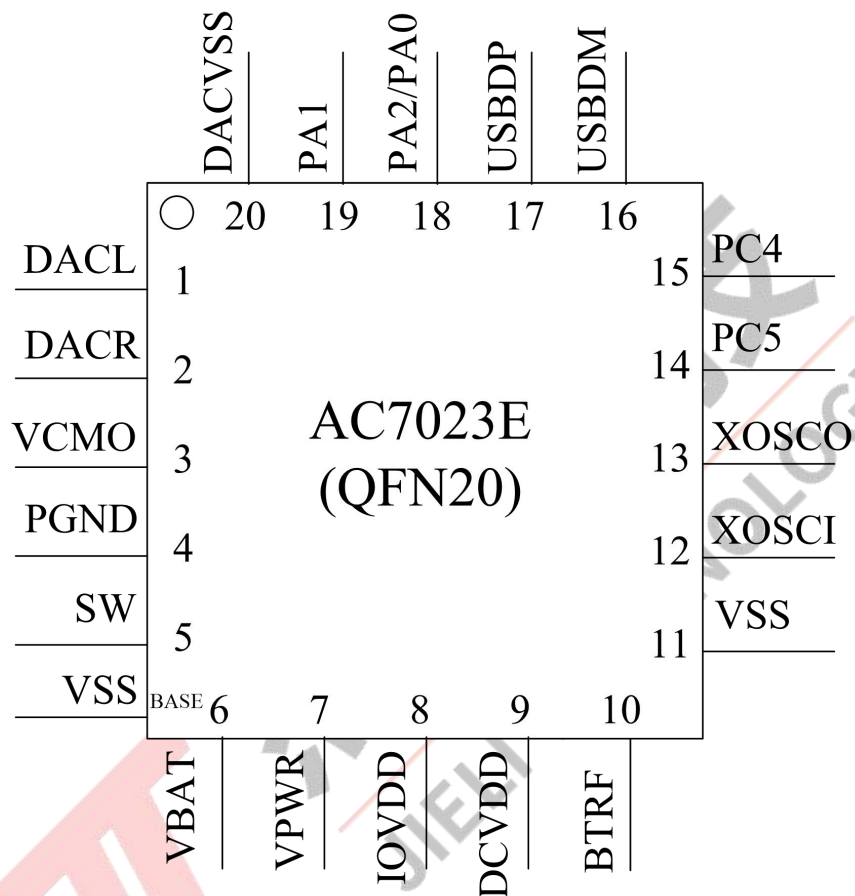


Figure 2-1 AC7023E Package Diagram

2.2 Pin Description

Table 2-1 AC7023E Pin Description

Pin No.	Pin name	Type	Function	Other function
1	DACL	AO	Analog Output	Left channel audio output positive;
2	DACR	AO	Analog Output	Right channel audio output positive;
3	VCMO	P		-
4	PGND	G		The ground of Buck DC-DC converter;
5	SW	PO		Switch signal of the Buck converter, connected to inductor;
6	VBAT	PI	GPIO	Battery interface;
7	VPWR (PP0)	PI (I/O)	GPIO (High Voltage Input)	Charge Power Input; UART0TXC: Uart0 Data Output(C); UART0RXC: Uart0 Data Input(C); PWM3: Timer3 PWM Output; CAP1: Timer1 Capture;
8	IOVDD	PO		IO Power;
9	DCVDD	P		DCDC power 1.25V;
10	BTRF	RFI		Bluetooth RF antenna interface;
11	VSS	G		Ground;
12	XOSCI	I		System Crystal Oscillator Input;
13	XOSCO	O		System Crystal Oscillator Output;
14	PC5	I/O	GPIO	IIC_SDA_B: IIC Data(B); ADC5 :ADC Input Channel 5; UART2RXD :Uart2 Data In(D);
15	PC4	I/O	GPIO	IIC_SCL_B: IIC Serial Clock(B); ADC4 : ADC Input Channel 4; UART2TXD: Uart2 Data Out(D); PWM4 :Timer4 PWM Output;
16	USBDM	I/O	USB Negative Data (pull down)	IIC_SDA_A: IIC SDA(A); ADC11: ADC Input Channel 11; UART1RXD: UART1 Data In(D);
17	USBDP	I/O	USB Positive Data (pull down)	IIC_SCL_A: IIC Clock(A); ADC10 :ADC Input Channel 10; UART1TXD :Uart1 Data Out(D);

18	PA2	I/O	GPIO	CLKOUT1: Clock Out1; MICBIAS0 : MIC0 Bias Output(Built-in resistor); UART1RXC :Uart1 Data In(C); CAP3: Timer3 Capture;
	PA0	I/O	GPIO	MICLDO : MIC0 Input Channel 0; UART2RXA :Uart2 Data In(A); CAP2: Timer2 Capture;
19	PA1	I/O	GPIO	MICIN0 :MIC0 Input Channel 0; UART1TXC :Uart1 Data Out(C); PWM0 :Timer0 PWM Output;
20	DACVSS	G		Ground;
BASE	VSS	G		Ground;

Pin Type	Description	Pin Type	Description
P	Power	I/O	Input or Output
PO	Power Output	I	Input
PI	Power Input	O	Output
G	Ground	RFI	Radio frequency interface
AO	Analog Output		

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1

Symbol	Parameter	Min	Max	Unit
T _{opt}	Operating temperature	-40	+85	°C
T _{stg}	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	4.5	V
VPWR	Charger Voltage	-0.3	6	V
V _{IOVDD}	Voltage applied at IOVDD	-0.3	3.6	V
V _{GPIO}	Voltage applied to GPIO	-0.3	IOVDD+0.3	V
V _{HVIO}	Voltage applied to High Voltage Resistant IO	-0.3	+5.5	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

3.2 PMU Characteristics

Table 3-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	4.5	V	
VPWR	Charger supply Voltage	4.5	5.0	5.5	V	
Operating mode						
IOVDD	Voltage output	–	3.0	–	V	VBAT = 4.2V, 10mA loading
	Loading current	–	–	200	mA	IOVDD=3.2V@VBAT = 3.5V
DCVDD	Voltage output	–	1.25	–	V	IOVDD=3.0V, 10mA loading
	Loading current	–	–	60	mA	DCVDD=1.25V@IOVDD=3.0v on LDO mode
		–	–	150	mA	DCVDD=1.25V@VBAT=3.0v on DCDC mode
Low Power mode						
IOVDD	Loading current	–	–	10	mA	IOVDD=3V@VBAT = 4.2V

3.3 Battery Charge

Table 3-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VPWR	Charge Input Voltage	4.5	5	5.5	V	–
V _{bat float}	Charge Voltage	4.15	4.2	4.25	V	VPWR > 4.5V
I _{bat}	Charge Current	20	–	200	mA	Charge current at fast charge mode VBAT=4.0V@VPWR=5.0V
I _{end}	End Of Charge Current	2	–	30	mA	End of charge current
V _{Trickl}	Trickle Charge Voltage	–	3.0	–	V	VPWR > 4.5V

3.4 IO Input/Output Electrical Logical Characteristics

Table 3-4

GPIO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Low-Level Input Voltage	-0.3	–	0.3* IOVDD	V	IOVDD = 3.0V
V _{IH}	High-Level Input Voltage	0.7* IOVDD	–	IOVDD+0.3	V	IOVDD = 3.0V
High Voltage Resistant IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Low-Level Input Voltage	-0.3	–	0.3* IOVDD	V	IOVDD = 3.0V
V _{IH}	High-Level Input Voltage	0.7* IOVDD	–	+5V	V	IOVDD = 3.0V
GPIO & High Voltage Resistant IO output characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{OL}	Low-Level Output Voltage	–	–	0.1* IOVDD	V	IOVDD = 3.0V
V _{OH}	High-Level Output Voltage	0.9* IOVDD	–	–	V	IOVDD = 3.0V

3.5 Internal Resistor Characteristics

Table 3-5

Port	Drive(mA)		Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA1,PA2 PC4,PC5	HD,HD0==0,0	2.4	10K	10K	1、PB1 default pull up 2、USBDM & USBDP default pull Down 3、internal pull-up / pull-down resistance accuracy ±20%
	HD,HD0==0,1	8			
	HD,HD0==1,0	26			
	HD,HD0==1,1	46			
PP0(VPWR)	8 (High Voltage Resistant)		10K	10K	
PA0	8		10K	10K	
USBDP	4		1.5K	15K	
USBDM			180K	15K	

3.6 Audio DAC Characteristics

Audio Format: SBC

Table 3-6

Parameter	Mode	Min	Typ	Max	Unit	Test Conditions
Frequency Response	Vcmo-Stereo	20	—	20k	Hz	1KHz/0dB 32 ohm loading With A-Weighted Filter
Output Swing	Vcmo-Stereo	—	0.35	0.68	Vrms	
THD+N	Vcmo-Stereo	—	-68	—	dB	
S/N	Vcmo-Stereo	—	95	98	dB	
Dynamic Range	Vcmo-Stereo	—	96	98	dB	1KHz/-60dB 32 ohm loading With A-Weighted Filter
Noise Floor	Vcmo-Stereo	—	6	—	uVrms	A-Weighted Filter
DAC Output Power	Vcmo-Stereo	—	7.8	14	mW	32ohm loading

3.7 Audio ADC Characteristics

Audio Filter: A-Weighted

Table 3-7

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range	—	85	—	dB	Fsample=44.1kHz,Gain=6dB Fin=1KHz 320mVrms
SNR	—	85	—	dB	Fsample=44.1kHz,Gain=6dB Fin=1KHz 320mVrms
THD+N	—	-70	—	dB	
SNR	—	77	—	dB	Fsample=44.1kHz,Gain=16dB Fin=1KHz 90mVrms
THD+N	—	-65	—	dB	

3.8 BT Characteristics

3.8.1 Transmitter

Basic Data Rate

Table 3-8

Parameter		Min	Typ	Max	Unit	Test Conditions
RF Transmit Power, DH5			6	8	dBm	25°C, Power Supply VBAT >=3.7V
RF Power Control Range, DH1			20		dB	
20dB Bandwidth, DH5			920		KHz	
Adjacent Channel Transmit Power, DH1 (BQB Test Mode RF_Tx Power=3.6dBm)	+2MHz		-53		dBm	
	-2MHz		-50		dBm	
	+3MHz		-55		dBm	
	-3MHz		-53		dBm	

Enhanced Data Rate

Table 3-9

Parameter		Min	Typ	Max	Unit	Test Conditions
Relative Power			-1.4		dB	25°C Power Supply VBAT >=3.7V
$\pi/4$ DQPSK Modulation Accuracy	DEVM RMS		6		%	
	DEVM 99%		11		%	
	DEVM Peak		16		%	
In-band spurious Emissions (BQB Test Mode RF_Tx Power=3.6dBm)	+2MHz		-42		dBm	2441MHz
	-2MHz		-38		dBm	2DH5
	+3MHz		-46		dBm	4 Layers Board
	-3MHz		-40		dBm	

3.8.2 Receiver

Basic Data Rate

Table 3-10

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-91		dBm	25°C, Power Supply VBAT >=3.7V
Co-channel Interference Rejection			4		dB	
Adjacent Channel Interference Rejection	+1MHz		-26		dB	
	-1MHz		-25		dB	
	+2MHz		-40		dB	
	-2MHz		-35		dB	
	+3MHz		-42		dB	
	-3MHz		-36		dB	

Enhanced Data Rate**Table 3-11**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity		-94	-92		dBm	25°C, Power Supply VBAT >=3.7V 2441MHz 2DH5 4 Layers Board
Co-channel Interference Rejection			10		dB	
Adjacent Channel Interference Rejection	+1MHz		-27		dB	
	-1MHz		-26		dB	
	+2MHz		-31		dB	
	-2MHz		-28		dB	
	+3MHz		-37		dB	
	-3MHz		-24		dB	

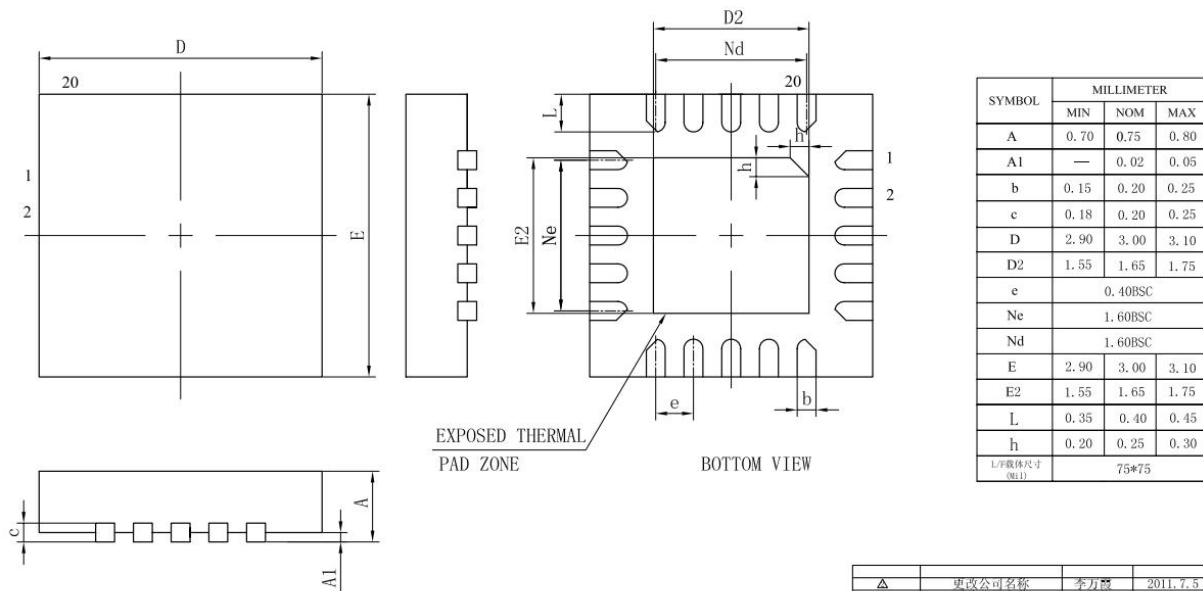
3.9 ESD Protection**Table 3-12**

Parameter	Typ.	Test pin	Reference standard
Human Body Mode	±4KV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	±200V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±1KV	All pins	JEDEC EIA/JESD22-C101F
Latch up	±200mA	All GPIO pins	JEDEC STANDARD NO.78E
	1.5xVopmax	All power pins	

Note : 1.5xVopmax = 1.5 times maximum operating voltage.

4 Package Information

4.1 QFN20_3.0x3.0



△	更改公司名称	李万露	2011.7.5
△	更改公司名称	李新锋	2011.3.3
更改标记	更改内容	签名	日期

Figure 4-1 AC7023E Package

5 Solder-Reflow Condition

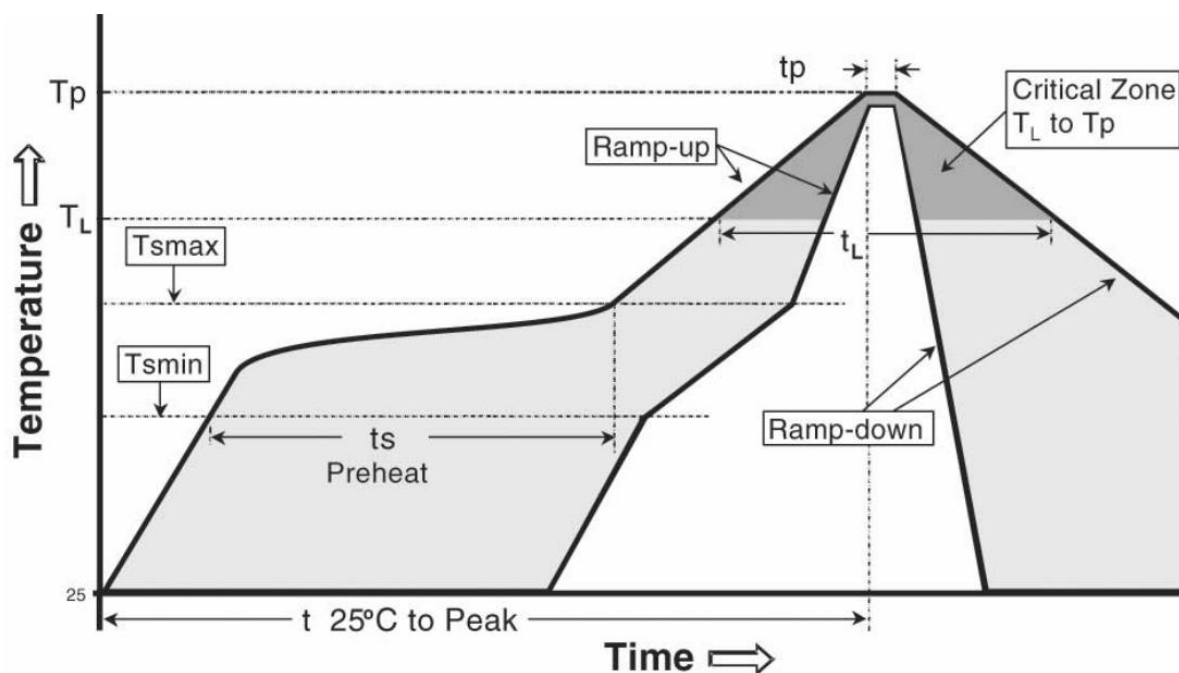


Figure 5-1 Classification Reflow Profile

Classification Profiles

Table 5-1

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/ Soak	Temperature Min (T_{smin})	100°C	150°C
	Temperature Max (T_{smax})	150°C	200°C
	Time (t_s) from (T_{smin} to T_{smax})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{smax} to T_p)		3°C/second max	3°C/second max
Liquidous temperature (T_L)		183°C	217°C
Time (t_L) maintained above T_L		60-150 seconds	60-150 seconds
Peak package body temperature (T_p)		See Table 5-2	See Table 5-3
Time within 5°C of actual Peak Temperature (t_p) ²		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6°C/second max	6°C/second max
Time 25°C to peak temperature		6 minutes max	8 minutes max

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5°C of actual peak temperature (t_p) specified for the reflow profiles is a “supplier” minimum and “user” maximum.

SnPb - Classification Temperature**Table 5-2**

Package Thickness	Volume mm ³	Volume mm ³
	< 350	≥ 350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Pb-free - Classification Temperature**Table 5-3**

Package Thickness	Volume mm ³	Volume mm ³	Volume mm ³
	< 350	350 - 2000	> 2000
< 1.6mm	260°C	260°C	260°C
1.6 mm - 2.5mm	260°C	250°C	245°C
> 2.5mm	250°C	245°C	245°C

*Tolerance: The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

6 Revision History

Date	Revision	Description
2022.09.06	V1.0	Initial Release
2022.12.20	V1.1	Update resource description
2023.12.18	V1.2	Update Feature_Bluetooth
2024.09.29	V1.3	Update Feature_Audio Codec Update Audio DAC Characteristics