

AD160A Datasheet

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AD160A Features

CPU

- 32bit DSP
- Maximum speed 160MHz
- Interrupts with 8 priority level

Memory

- OTP
- Optional built-in flash memory

Clocks

- On-chip 16 MHz clock
- On-chip 200KHz lower-temperature-drift clock
- 12 MHz crystal oscillator
- 32.768 KHz crystal oscillator

DSP Audio Processing

- Support MP2, MP3, WMA, WAV decoding
- Multi-band DRC limiter
- Multi-band EQ configuration for voice Effects

Audio Codec

- Two channels 16-bit DAC, single-ended with SNR \geq 97dB, differential with SNR \geq 100dB
- One channel 24-bit ADC, SNR \geq 88dB
- Audio DAC Sampling rates of 8KHz/11.025KHz/16KHz/22.05KHz/24KHz/32KHz/44.1KHz/48KHz/64KHz/88.2KHz/96KHz are supported
- Audio ADC Sampling rates of 8KHz/11.025KHz/16KHz/22.05KHz/24KHz/32KHz/44.1KHz/48KHz are supported
- Audio DAC support single-ended and differential cap-less mode
- Support analog audio input
- Support OMTP and CTIA earphone plug-in and pull-out detection
- Support for driving 16 or 32 ohm speaker

Peripherals

- One full speed USB OTG controller
- One SD host controller for MMC/SD
- Three multi-function 32-bit timers, support capture and PWM mode
- UART0 controller
- The UART1 supports DMA and flow control
- One IIC Master controller
- Two SPI Master / Slaver controller with DMA
- One QDEC interface
- 16-channel 10-bit general purpose ADC
- 4-channel Advance PWM controller
- LCD controller
- A0:38 Individually programmable and multiplexed GPIO pins
- A2/A4:33 Individually programmable and multiplexed GPIO pins
- Digital peripheral crossbar
- Up to 12 external interrupt / wake-up source (low power available, can be multiplexed to any I/O)

PMU

- Built-in lithium battery charging manager, up to 120mA charging current
- RTC Alarm Wakeup
- Less than 2uA soft off current
- VPWR range : 4.5V to 6.0V
- VBAT range : 2.2V to 5.0V
- IOVDD range : 2.1V to 3.6V

Packages

- QFN52(6mm*6mm)

Temperature

- Operating temperature: -40°C to +85°C
- Storage temperature: -65°C to +150°C

Applications

- Audio player
- Microcontrollers

1 Block Diagram

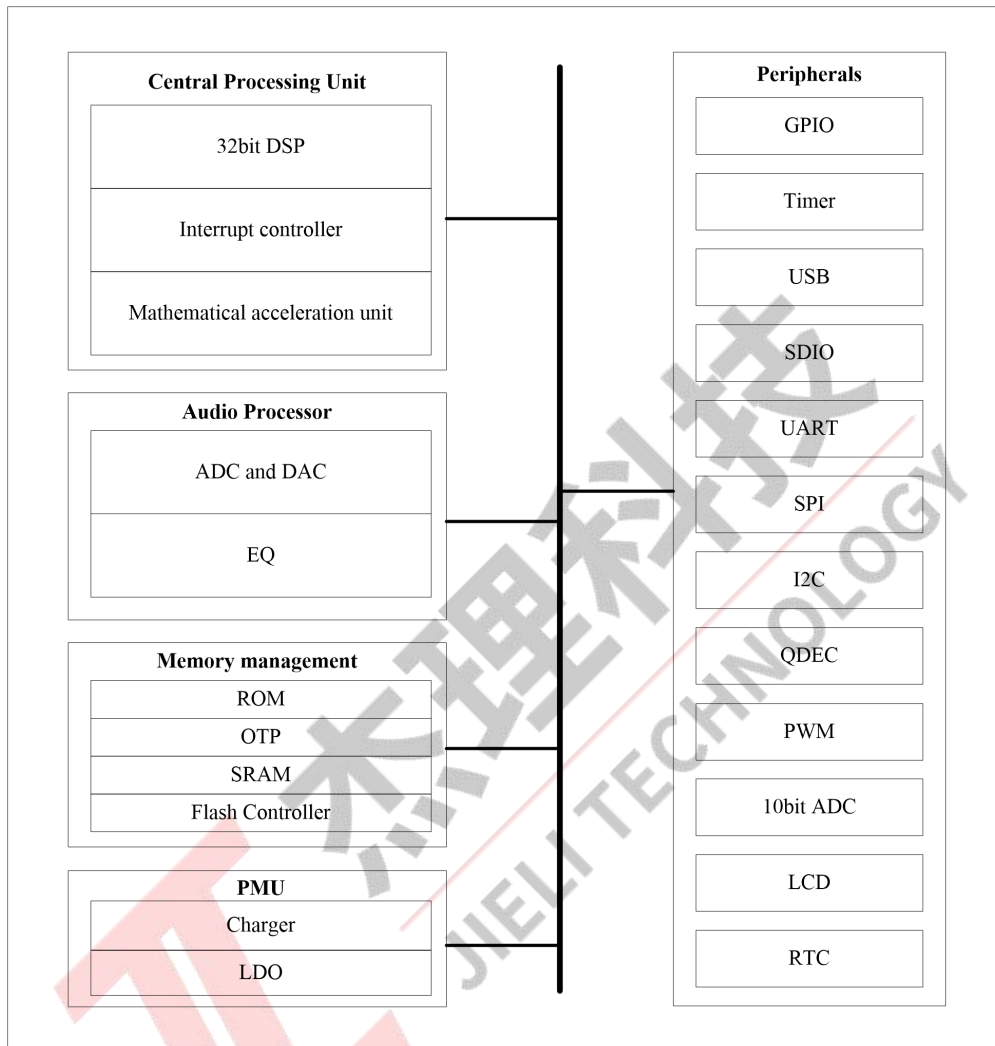


Figure 1-1 AD160A Block Diagram

2 Pin Definition

2.1 Pin Assignment

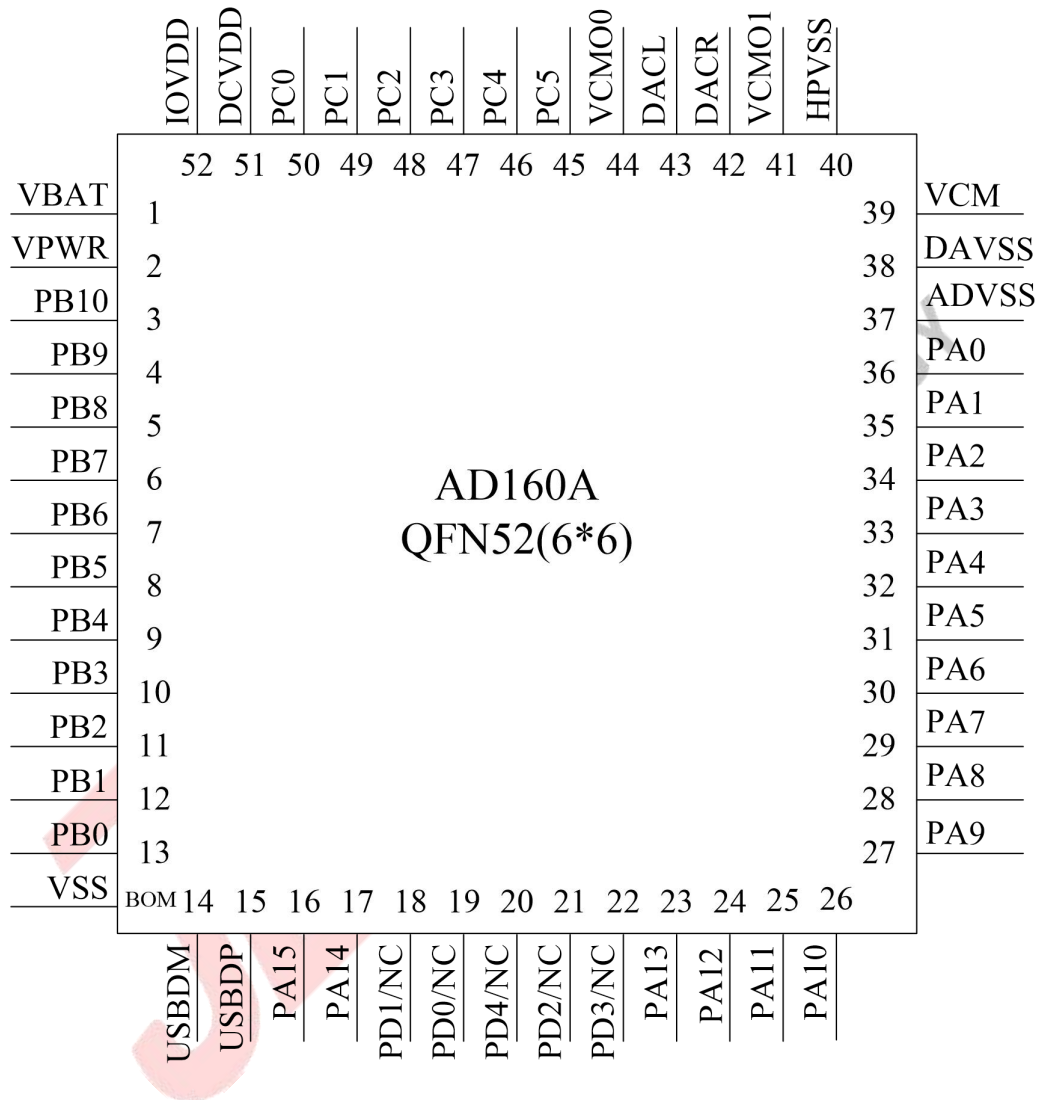


Figure 2-1 AD160A Package Diagram

2.2 Pin Description

Table 2-1 AD160A Pin Description

PIN NO.	Name		Type	Function	Other Function
	A0	A2/A4			
1	VBAT		P		Battery interface;
2	VPWR (PP0)		PI (I/O)	GPIO	Charge Power Input; UART1TXA:Uart1 Data Output(A); UART1RXA:Uart1 Data Input(A); CAP1:Timer1 Capture;
3	PB10		I/O	GPIO	PPS_DAT:Power protocol slave control; CLKOUT3:Clock Out3;
4	PB9		I/O	GPIO	ROSCI_32K:32.768KHz crystal oscillator input; CLKOUT2:Clock Out2; LCD SEG25;
5	PB8		I/O	GPIO	ROSCO_32K:32.768KHz crystal oscillator output; Q-decoder_1; IIC0_SDA(B):IIC0 SDA(B); ADC10:ADC Input Channel 10; CLKOUT1:Clock Out1; LCD SEG24;
6	PB7		I/O	GPIO	Q-decoder_0; IIC0_SCL(B):IIC0 SCL(B); ADC9:ADC Input Channel 9; CLKOUT0:Clock Out0; LCD SEG23;
7	PB6		I/O	GPIO	OSC12MO:12MHz crystal oscillator output; ADC8:ADC Input Channel 8; LCD SEG22;
8	PB5		I/O	GPIO	OSC12MI:12MHz crystal oscillator input; LCD SEG21;
9	PB4		I/O	GPIO	SPI1DI(B):SPI1 Data In(B); SDDAT(A):SD Data(A); ADC7:ADC Input Channel 7; LCD SEG20;
10	PB3		I/O	GPIO	SPI1DO(B):SPI1 Data Out(B); SDCMD(A/B):SD CMD(A/B); CAP2:Timer2 Capture; LCD SEG19;

11	PB2		I/O	GPIO	SPI1CLK(B):SPI1 Clk(B); SDCLK(A/B):SD Clock(A/B); ADC6:ADC Input Channel 6; LCD SEG18;
12	PB1		I/O	GPIO	SPI1DI(A):SPI1 Data In(A); LCD SEG17;
13	PB0		I/O	GPIO	ADC5:ADC Input Channel 5; LCD SEG16;
14	UDBDM		I/O	USB Negative Data (pull down)	SDDAT(B):SD Data(B); SPI1DO(A):SPI1 Data Out(A); IIC0_SDA(A):IIC0 SDA(A); UART0RXA:Uart0 Data Input(A); ADC15:ADC Input Channel 15;
15	USBDP		I/O	USB Positive Data (pull down)	SPI1CLKA:SPI1 Clk(A); IIC0_SCL(A):IIC0 SCL(A); UART0TXA:Uart0 Data Output(A); ADC14:ADC Input Channel 14;
16	PA15		I/O	GPIO	PWM1:Timer1 PWM Output; LCD SEG15;
17	PA14		I/O	GPIO (pull down)	LCD SEG14;
18	PD1	NC	I/O	GPIO	SFCDO(A):SFC Data Out(A); SPI0DO(A):SPI0 Data Out(A); LCD SEG28;
19	PD0	NC	I/O	GPIO	SFCCLK(A):SFC Clk(A); SPI0CLK(A):SPI0 Clk(A); LCD SEG27;
20	PD4	NC	I/O	GPIO	LCD SEG31; Flash Power Gate;
21	PD2	NC	I/O	GPIO	SFCDI(A):SFC Data In(A); SPI0DI(A):SPI0 Data In(A); LCD SEG29;
22	PD3	NC	I/O	GPIO	SFCCS(A):SFC Chip Select(A); SPI0CS(A):SPI0 Chip Select(A); LCD SEG30;
23	PA13		I/O	GPIO (pull down)	LCD SEG13;
24	PA12		I/O	GPIO	SDCLK(C):SD Clock(C); FPIN1; TMR1:Timer1 Clock Input; LCD SEG12;

25	PA11	I/O	GPIO	SDCMD(C):SD CMD(C); M_TMR1CK; LCD SEG11;
26	PA10	I/O	GPIO	SDDAT(C):SD Data(C); ADC4:ADC Input Channel 4; PWMCH1L:Motor PWM Channel1(L); LCD SEG10;
27	PA9	I/O	GPIO	PWMCH1H:Motor PWM Channel1(H); LCD SEG9;
28	PA8	I/O	GPIO (pull up)	Long press reset; ADC3:ADC Input Channel 3; LCD SEG8;
29	PA7	I/O	GPIO	LCD SEG7; LCD COM0(B);
30	PA6	I/O	GPIO	ADC2:ADC Input Channel 2; LCD SEG6; LCD COM1(B);
31	PA5	I/O	GPIO	PPM_DAT0:Power protocol master control 0; FPIN0; LCD SEG5; LCD COM2(B);
32	PA4	I/O	GPIO	M_TMR0CK; ADC1:ADC Input Channel 1; CAP0:Timer0 Capture; LCD SEG4; LCD COM3(B);
33	PA3	I/O	GPIO	PPM_DAT1:Power protocol master control 1; UART1_RTS:Uart1 request to send; PWMCH0L:Motor PWM Channel0(L); LCD SEG3; LCD COM4(B);
34	PA2	I/O	GPIO	MICIN1:MIC1 Input Channe; UART1_CTS:Uart1 clear to send; PWMCH0H:Motor PWM Channel0(H); LCD SEG2; LCD COM5(B);
35	PA1	I/O	GPIO	MICIN0:MIC0 Input Channe; UART1RXB:Uart1 Data Input(B); TMR0:Timer0 Clock Input; LCD SEG1;

36	PA0	I/O	GPIO	MICLDO:Microphone linear voltage regulator output; ADC0:ADC Input Channel 0; UART1TXB:Uart1 Data Output(B); PWM0:Timer0 PWM Output; LCD SEG0;
37	ADVSS	G		Audio ADC ground;
38	DAVSS	G		Audio DAC ground;
39	VCM	P		Audio analog reference bias;
40	HPVSS	G		Headphone AMP ground;
41	VCMO1	AO		Reference output1 of the audio;
42	DACR	AO		Right channel audio output;
43	DACL	AO		Left channel audio output;
44	VCMO0	AO		Reference output0 of the audio;
45	PC5	I/O	GPIO	AINR:Right channel analog audio input; LCD COM0(A);
46	PC4	I/O	GPIO	AINL:Left channel analog audio input; SFCSS(B):SFC Chip Select(B); SPI0CS(B):SPI0 Chip Select(B); TMR2:Timer2 Clock Input; LCD COM1(A);
47	PC3	I/O	GPIO	SFCDI(B):SFC Data In(B); SPI0DI(B):SPI0 Data In(B); SDPG:SD card Power Gate; ADC13:ADC Input Channel 13; LCD COM2(A);
48	PC2	I/O	GPIO	SDCLK(D):SD Clock(D); LCD COM3(A);
49	PC1	I/O	GPIO	SFCCLK(B):SFC Clk(B); SPI0CLK(B):SPI0 Clk(B); SDCMD(D):SD CMD(D); UART0RXB:Uart0 Data Input(B); ADC12:ADC Input Channel 12; LCD COM4(A);
50	PC0	I/O	GPIO	SFCDO(B):SFC Data Out(B); SPI0DO(B):SPI0 Data Out(B); SDDAT(D):SD Data(D); UART0TXB:Uart0 Data Output(B); PWM2:Timer2 PWM Output; ADC11:ADC Input Channel 11; LCD SEG26; LCD COM5(A);
51	DCVDD	P		Internal power;

52	IOVDD	PO	Power supply for GPIO	Built-in linear voltage regulator output;
BOM	VSS	G		System ground;

Pin Type	Description	Pin Type	Description
P	Power	I/O	Input or Output
PI	Power Input	I	Input
PO	Power Output	O	Output
AO	Analog Output	G	Ground



3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1

Symbol	Parameter	Min	Max	Unit
T _{opt}	Operating temperature	-40	+85	°C
T _{stg}	Storage temperature	-65	+150	°C
V _{BAT}	Supply Voltage	-0.3	5.0	V
V _{PWR}	Charger Voltage	-0.3	6.0	V
V _{IOVDD}	Voltage applied at IOVDD	-0.3	3.6	V
V _{GPIO}	Voltage applied to GPIO	-0.3	IOVDD+0.3	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

3.2 PMU Characteristics

Table 3-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{BAT}	Voltage Input	2.2	3.7	5.0	V	—
V _{PWR}	Charger supply Voltage	4.5	5.0	6.0	V	—
DCVDD	Voltage output	1.14	1.35	1.59	V	—
IOVDD	Voltage output	2.1	3.0	3.6	V	V _{BAT} = 4.2V, 10mA loading
	Loading current	—	—	100	mA	IOVDD=3.3V@V _{BAT} = 3.6V
V _{LVD}	Voltage input	2.1	2.8	2.8	V	Low-Voltage Detection of IOVDD

3.3 Battery Charge

Table 3-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{PWR}	Charge Input Voltage Range	4.5	5	6.0	V	—
V _{BAT Float}	Battery Charge Termination Voltage	4.15	4.2	4.25	V	VPWR>4.5V
		4.30	4.35	4.40	V	VPWR>4.65V
I _{BAT}	Fast Charge Current	20	—	120	mA	V _{BAT} =4.0V@VPWR=5.0V
I _{END}	Charge Termination Current Threshold	2	—	12	mA	CHG_IIFULL_S=0,1
V _{Trickl}	Trickle Charge Voltage	—	3.0	—	V	VPWR>4.5V
I _{Trickl}	Trickle Charge Current	2	—	12	mA	V _{BAT} <V _{Trickl}

3.4 IO Input/Output Electrical Logical Characteristics

Table 3-4

GPIO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Low-Level Input Voltage	-0.3	–	0.3* IOVDD	V	IOVDD = 3.0V
V _{IH}	High-Level Input Voltage	0.7* IOVDD	–	IOVDD+0.3	V	IOVDD = 3.0V
GPIO output characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{OL}	Low-Level Output Voltage	–	–	0.1* IOVDD	V	IOVDD = 3.0V
V _{OH}	High-Level Output Voltage	0.9* IOVDD	–	–	V	IOVDD = 3.0V

3.5 Internal Resistor Characteristics

Table 3-5

Port	Drive Current	Internal Pull-Up Resistor		Internal Pull-Down Resistor	Comment
PA0~PA2,PA4 PA6~PA15 PB0~PB9 PC0~PC5 PD0~PD4	2mA(HD1,HD0==0,0) 5.6mA(HD1,HD0==0,1) 18mA(HD1,HD0==1,0) 30mA(HD1,HD0==1,1)	10K		10K	1. PA8 default pull up 2. USBDM,USBDP,PA13,PA14 default pull down 3. Internal pull-up/pull-down resistance accuracy ±20%
PA3,PA5		PU	10K	10K	
		PU1	0.2K		
PB10	27mA	10K		10K	
PP0(VPWR)	1.4mA	10K		10K	
USBDP	27mA	1.5K		15K	
USBDM		180K		15K	

3.6 Audio DAC Characteristics

Table 3-6

Parameter	MODE	Min	Typ	Max	Unit	Test Conditions
Frequency Response		20	–	20K	Hz	1KHz/0dB 10k ohm loading With A-Weighted Filter IOVDD>2.7V
Output Swing	Diff (R to L)	–	1.5	–	Vrms	
	Single-ended	–	750	–	mVrms	
THD+N	Diff (R to L)	–	-80	–	dB	
	Single-ended	–	-80	–	dB	
S/N	Diff (R to L)	–	100	–	dB	
	Single-ended	–	97@VCM cap 93@VCM capless	–	dB	
Dynamic Range	Diff (R to L)	–	100	–	dB	
	Single-ended	–	97@VCM cap 93@VCM capless	–	dB	
Noise Floor	Diff (R to L)	–	13	–	uVrms	
	Single-ended	–	11@VCM cap 18@VCM capless	–	uVrms	
Crosstalk	Single-ended	–	-93	–	dB	10KHz/0dB 10k ohm loading IOVDD>2.7V
	(R and L) to VCMO	–	-60	–	dB	10KHz/0dB 32 ohm loading IOVDD>2.7V
	(R and L) to VCMO	–	-57	–	dB	10KHz/0dB 16 ohm loading IOVDD>2.7V

3.7 Audio ADC Characteristics

Table 3-7

Parameter	MODE	Min	Typ	Max	Unit	Test Conditions
Dynamic Range	Differential	–	88	–	dB	Fsample=44.1KHz, Gain=4dB Fin=1KHz @1Vpp NO A-wt 20Hz-20KHz IOVDD>2.7V
		–	83	–	dB	Fsample=44.1KHz, Gain=20dB Fin=1KHz @160mVpp NO A-wt 20Hz-20KHz IOVDD>2.7V

Dynamic Range	Single-ended	-	88@VCM cap 85@VCM capless	-	dB	Fsample=44.1KHz,Gain=-2dB Fin=1KHz @1Vpp NO A-wt 20Hz-20KHz IOVDD>2.7V
		-	76@VCM cap 72@VCM capless	-	dB	Fsample=44.1KHz,Gain=14dB Fin=1KHz @160mVpp NO A-wt 20Hz-20KHz IOVDD>2.7V
S/N	Differential	-	88	-	dB	Fsample=44.1KHz,Gain=4dB Fin=1KHz @1Vpp NO A-wt 20Hz-20KHz IOVDD>2.7V
		-	80	-	dB	Fsample=44.1KHz,Gain=20dB Fin=1KHz @160mVpp NO A-wt 20Hz-20KHz IOVDD>2.7V
	Single-ended	-	88@VCM cap 85@VCM capless	-	dB	Fsample=44.1KHz,Gain=-2dB Fin=1KHz @1Vpp NO A-wt 20Hz-20KHz IOVDD>2.7V
		-	76@VCM cap 72@VCM capless	-	dB	Fsample=44.1KHz,Gain=14dB Fin=1KHz @160mVpp NO A-wt 20Hz-20KHz IOVDD>2.7V
THD+N	Differential	-	-80	-	dB	Fsample=44.1KHz,Gain=4dB Fin=1KHz @1Vpp NO A-wt 20Hz-20KHz IOVDD>2.7V
		-	-78	-	dB	Fsample=44.1KHz,Gain=20dB Fin=1KHz @160mVpp NO A-wt 20Hz-20KHz IOVDD>2.7V
	Single-ended	-	-79@VCM cap -78@VCM capless	-	dB	Fsample=44.1KHz,Gain=-2dB Fin=1KHz @1Vpp NO A-wt 20Hz-20KHz IOVDD>2.7V
		-	-72@VCM cap -70@VCM capless	-	dB	Fsample=44.1KHz,Gain=14dB Fin=1KHz @160mVpp NO A-wt 20Hz-20KHz IOVDD>2.7V

4 Package Information

4.1 QFN52_6×6mm

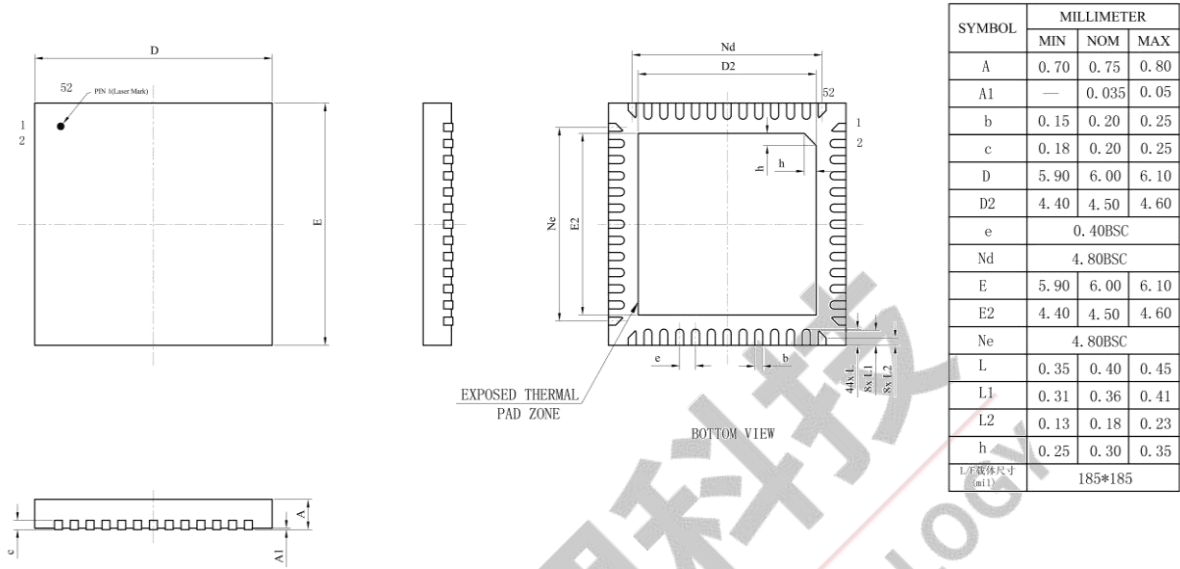
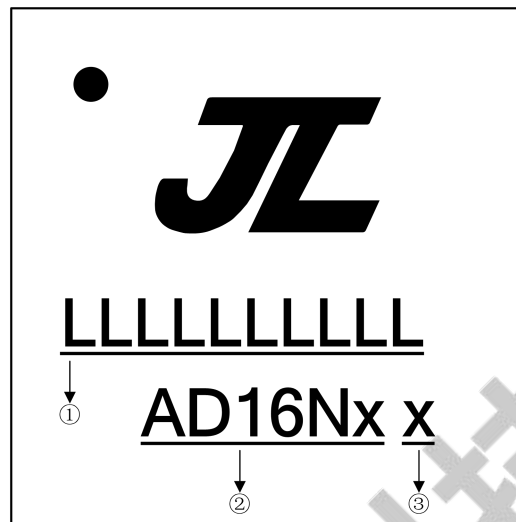


Figure 4-1 AD160A Package

5 IC Marking Information



① LLLLLLLLLL : Production Batch

② AD16Nx : Chip Model

③ Built-in flash size

0: No Flash Memory

2: 2Mbit Flash

4: 4Mbit Flash

8: 8Mbit Flash

6: 16Mbit Flash

3: 32Mbit Flash

6 Solder-Reflow Condition

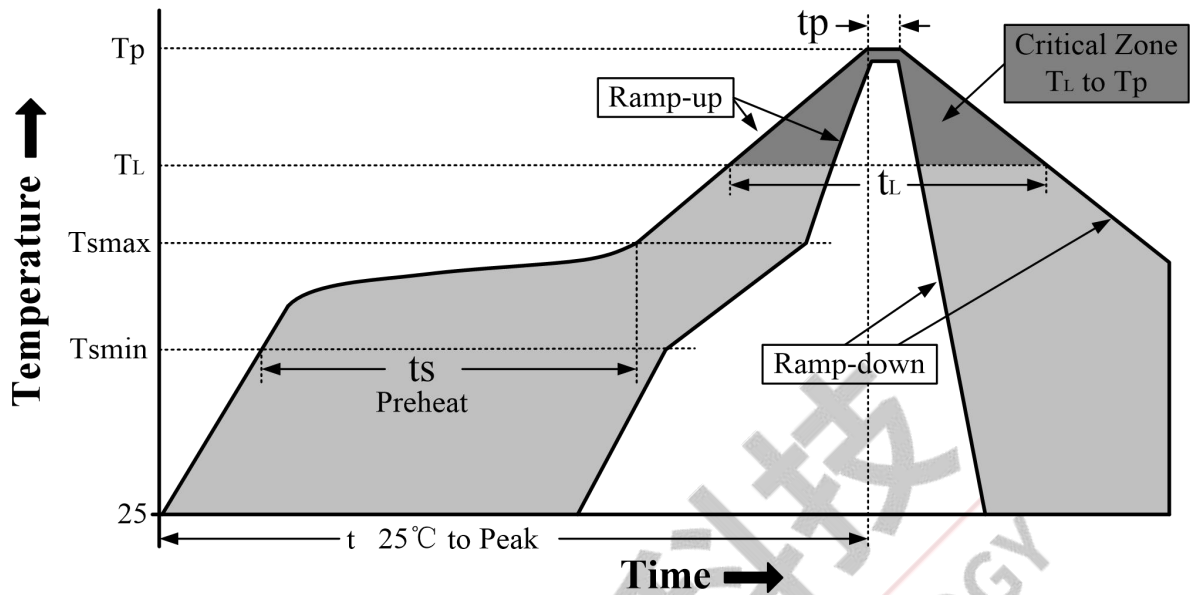


Figure 6-1 Classification Reflow Profile

Classification Profiles

Table 6-1

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/ Soak	Temperature Min (T_{smin})	100 °C	150 °C
	Temperature Max (T_{smax})	150 °C	200 °C
	Time (t_s) from (T_{smin} to T_{smax})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{smax} to T_p)		3 °C/second max	3 °C/second max
Liquidous temperature (T_L)		183 °C	217 °C
Time (t_L) maintained above T_L		60-150 seconds	60-150 seconds
Peak package body temperature (T_p)		See Table 6-2.	See Table 6-3.
Time within 5°C of actual Peak Temperature (t_p)		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature		6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5°C of actual peak temperature (t_p) specified for the reflow profiles is a “supplier” minimum and “user” maximum.

SnPb - Classification Temperature

Table 6-2

Package Thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
<2.5 mm	240 +0/-5 °C	225 +0/-5 °C
≥ 2.5 mm	225 +0/-5 °C	225 +0/-5 °C

Pb-free - Classification Temperature **Table 6-3**

Package Thickness	Volume mm³ < 350	Volume mm³ 350 - 2000	Volume mm³ > 2000
< 1.6mm	260 °C	260 °C	260 °C
1.6 mm - 2.5mm	260 °C	250 °C	245 °C
> 2.5mm	250 °C	245 °C	245 °C



7 Revision History

Date	Revision	Description
2022.09.16	V1.0	Initial Release.
2022.11.28	V1.1	Update Pin Definition. Update VPWR,VBAT range. Update DAC,ADC Characteristics.
2023.03.22	V1.2	Features modification

