

AC6321A Datasheet

Zhuhai Jieli Technology Co.,LTD

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AC6321A Features

High performance 32-bit RISC CPU

- RISC 32-bit CPU
- DC-96MHz operation
- 73KB data RAM
- 8KB I-cache 2way
- 1KB Rocache 1way
- 64 Vectored interrupts
- 8 Levels interrupt priority

Flexible I/O

- 25 GPIO pins
- All GPIO pins can be programmable as input or output individually
- All GPIO pins are internal pull-up/pull-down selectable individually
- CMOS/TTL level schmitt triggered input
- External wake up/interrupt on all GPIOs

Peripheral Feature

- Two Full Speed USB OTG controller
- Four Multi-function 32-bit timers, support capture and PWM mode
- Three full-duplex advanced UART(DMA)
- Three SPI interface supports host and device mode (DMA)
- One IIC interface supports host and device mode
- RTC,with alarm clock and time base to wake up the chip
- 16-bit PWM generator for motor driving
- Three IQ Encoder
- 16 channels 10-bit ADC
- 1 channel 8 levels Low Power Detector

- Embedded PMU support low power mode
- 2 Crystal Oscillator
- Watchdog
- Power-on reset

Bluetooth Feature

- CMOS single-chip fully-integrated radio and baseband
- Dual-mode BT6.0 (DN Q334307)
- Bluetooth Piconet and Scatternet support
- Meet class2 and class3 transmitting power requirement
- Support GFSK and $\pi/4$ DQPSK all packet types
- Maximum +8dBm transmitting power
- EDR receiver with -93dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smpl\att\gap\gatt\rfcomm\sdp\l2cap profile

Power Supply

- LDOIN is 4.5V to 5.5V
- VBAT is 1.8V to 4.5V
- VDDIO is 1.8V to 3.4V

Packages

- QFN32(4x4mm)

Temperature

- Operating temperature
TC=-20°C to +85°C (standard range)
TC=-40°C to +105°C (extended range)
- Storage temperature: -65°C to +150°C

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1. Block Diagram

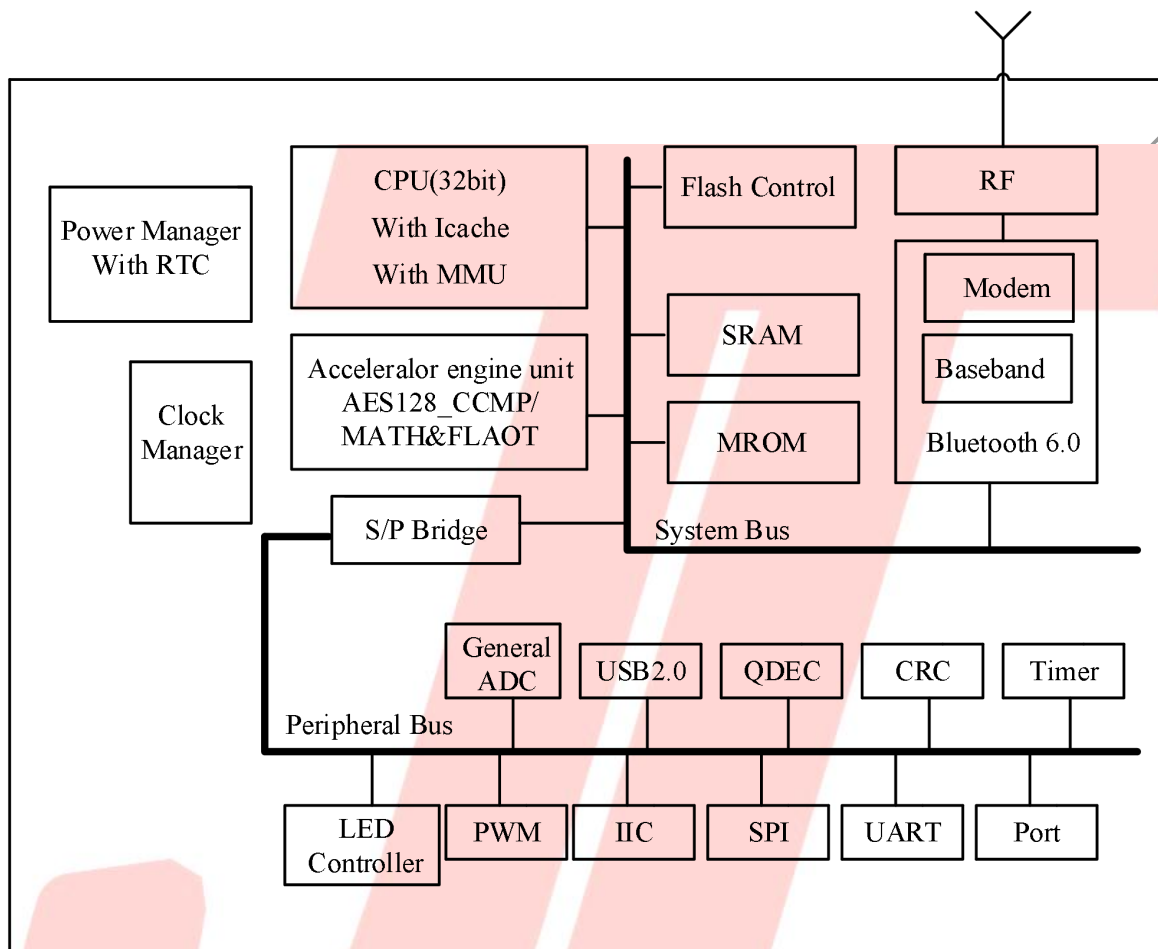


Figure 1-1 AC6321A_QFN32 Block Diagram

2. Pin Definition

2.1 Pin Assignment

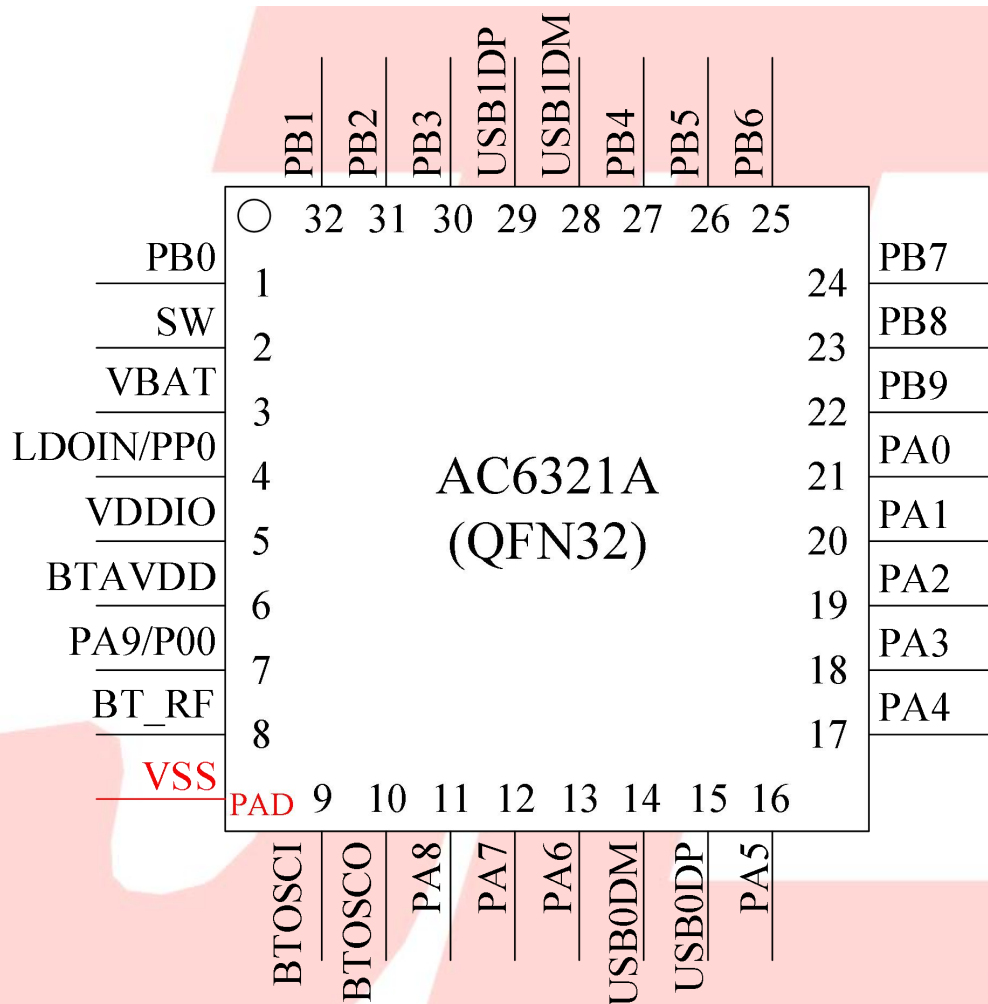


Figure 2-1 AC6321A_QFN32 Package Diagram

2.2 Pin Description

Table 2-1 AC6321A_QFN32 Pin Description

PIN NO.	Name	I/O Type	Function	Other Function
1	PB0	I/O	GPIO (High Voltage)	CLKOUT0; UART1_TXB: Uart1 Data Out(B); TMR2CK;
2	SW	P	DC-DC Switch Pin	-
3	VBAT	P	LDO Power	-
4	LDOIN/PP0	P	Charge Power 5V	PWM3: Timer3 PWM Output; UART0_TXD: Uart0 Data Out(D); UART0_RXD: Uart0 Data In(D);
5	VDDIO	P	IO Power 3.3V	-
6	BTAVDD	P	Core Power 1.3V	-
7	PA9	I/O	GPIO (pull up)	Long Press Reset; ADC8: ADC Channel 8;
	P00	I/O	GPIO (High Voltage)	
8	BT_RF	-	RF Antenna	-
9	BTOSCI	I	BTOSCI	-
10	BTOSCO	O	BTOSCO	-
11	PA8	I/O	GPIO	TMR3: Timer3 Clock In; SPI1_DOA: SPI1 Data Out(A); IIC_SDA_C: IIC SDA(C); ADC4: ADC Channel 4; UART1_RXC: Uart1 Data In(C); PWMCH1L;
12	PA7	I/O	GPIO	TMR1: Timer1 Clock In; SPI1_CLKA: SPI1 Clock(A) ; IIC_SCL_C: IIC SCL(C); ADC3: ADC Channel 3; UART1_TXC: Uart1 Data Out(C); PWMCH1H;

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13	PA6	I/O	GPIO	CAP0: Timer0 Capture; SPI1_DIA: SPI1 Data In(A); UART0_RXA: Uart0 Data In(A); TMR1CK;
14	USB0DM	I/O	GPIO (pull down)	SPI2_DOB: SPI2 Data Out(B); IIC_SDA_A: IIC SDA(A); ADC11: ADC Channel 11; UART1_RXD: Uart1 Data In(D);
15	USB0DP	I/O	GPIO (pull down)	SPI2_CLKB: SPI2 Clock(B); IIC_SCL_A: IIC SCL(A); ADC10: ADC Channel 10; UART1_TXD: Uart1 Data Out(D);
16	PA5	I/O	GPIO	TMR0: Timer0 Clock In; SPI2_DIB: SPI2 Data In(B); ADC2: ADC Channel 2; UART0_TXA: Uart0 Data Out(A); TMR0CK;
17	PA4	I/O	GPIO	PWM1: Timer1 PWM Output; IIC_SDA_D: IIC SDA(D); UART2_RXA: Uart2 Data In(A);
18	PA3	I/O	GPIO	CAP2: Timer2 Capture; IIC_SCL_D: IIC SCL(D); ADC1: ADC Channel 1; UART2_TXA: Uart2 Data Out(A); PWMCH0L;
19	PA2	I/O	GPIO	CAP3: Timer3 Capture; Q-decoder0_1; UART0_RXC: Uart0 Data In(C); UART1_RTS;
20	PA1	I/O	GPIO	PWM0: Timer0 PWM Output; Q-decoder0_0; ADC0: ADC Channel 0; UART0_TXC: Uart0 Data Out(C); UART1_CTS;
21	PA0	I/O	GPIO (High Voltage)	CLKOUT1; UART2_TXB: Uart2 Data Out(B); UART2_RXB: Uart2 Data In(B); PWMCH0H;
22	PB9	I/O	GPIO	32K_OSCI;
23	PB8	I/O	GPIO	32K_OSCO;
24	PB7	I/O	GPIO (High Voltage)	SPI2_DOA: SPI2 Data Out(A); UART2_RXC: Uart2 Data In(C);

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25	PB6	I/O	GPIO	SPI2_CLKA: SPI2 Clock(A) ; ADC12: ADC Channel 12; UART2_TXC: Uart2 Data Out(C); TMR3CK;
26	PB5	I/O	GPIO (High Voltage)	SPI2_DIA: SPI2 Data In(A); UART1_RXA: Uart1 Data In(A); PWMCH3L;
27	PB4	I/O	GPIO	TMR2: Timer2 Clock In; Q-decoder2_0; SPI1_DIB: SPI1 Data In(B); ADC9: ADC Channel 9; UAR1_TXA: Uart1 Data Out(A); PWMCH3H;
28	USB1DM	I/O	GPIO (pull down)	SPI1_DOB: SPI1 Data Out(B) ; IIC_SDA_B: IIC SDA(B); ADC6: ADC Channel 6; UART2_RXD: Uart2 Data In(D);
29	USB1DP	I/O	GPIO (pull down)	SPI1_CLKB: SPI1 Clock(B) ; IIC_SCL_B: IIC SCL(B); ADC5: ADC Channel 5; UART2_TXD: Uart2 Data Out(D);
30	PB3	I/O	GPIO (High Voltage)	UART0_RXB: Uart0 Data In(B); PWMCH2L; Q-decoder1_1;
31	PB2	I/O	GPIO (pull up)	MCLR; UART0_TXB: Uart0 Data Out(B); PWMCH2H; Q-decoder1_0;
32	PB1	I/O	GPIO (pull up)	PWM2: Timer2 PWM Output; ADC7: ADC Channel 7; UART1_RXB: Uart1 Data In(B); LVD;
PAD		P	GND	-

Note : Weak anti-static ability of PA9, need to take ESD protection measures when using.

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3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1

Symbol	Parameter	Min	Max	Unit
T _{opt}	Operating temperature	-40	+85	°C
T _{stg}	Storage temperature	-65	+150	°C
V _{BAT}	Supply Voltage	-0.3	4.5	V
LDOIN	Charge Input Voltage	-0.3	6	V
VDDIO	3.3V IO Input Voltage	-0.3	3.6	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

3.2 Recommended Operating Conditions

Table 3-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{BAT}	Voltage Input	1.8	3.7	4.5	V	—
LDOIN	Voltage Input	4.5	5.0	5.5	V	—
VDDIO	Voltage output	1.8	3.0	3.4	V	V _{BAT} = 4.2V, 60mA loading
BTAVDD	Voltage output	1	1.3	1.4	V	DC-DC mode: 40mA loading
I _{VDDIO}	Loading current	—	—	60	mA	V _{BAT} = 4.2V

3.3 Battery Charge

Table 3-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
LDOIN	Charge Input Voltage	4.5	5	5.5	V	—
V _{Charge}	Charge Voltage	4.15	4.2	4.25	V	—
I _{Charge}	Charge Current	20		200	mA	Charge current at fast charge mode
I _{Trinkl}	Trickle Charge Current	20	45	70	mA	V _{BAT} < V _{Trinkl}

3.4 IO Input/Output Electrical Logical Characteristics

Table 3-4

IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Low-Level Input Voltage	-0.3	—	$0.3 * V_{DDIO}$	V	$V_{DDIO} = 3.3V$
V_{IH}	High-Level Input Voltage	$0.7 * V_{DDIO}$	—	$V_{DDIO} + 0.3$	V	$V_{DDIO} = 3.3V$
IO output characteristics						
V_{OL}	Low-Level Output Voltage	—	—	0.33	V	$V_{DDIO} = 3.3V$
V_{OH}	High-Level Output Voltage	2.7	—	—	V	$V_{DDIO} = 3.3V$

3.5 Internal Resistor Characteristics

Table 3-5

Port	Drive Strength	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA1-PA9, PB1-PB2, PB4,PB6, PB8,PB9	drive_select[11] 24mA drive_select[10] 24mA (with 120ohm res) drive_select[01] 8mA drive_select[00] 8mA (with 120ohm res)	10K	10K	1. PA9&PB2 default pull up 2. USB0DM&USB0DP default pull down 3. USB1DM&USB1DP default pull down 4. Internal pull-up/pull-down resistance accuracy $\pm 20\%$ 5. PA0,PB0,PB3,PB5,PB7,P00,PP0 can pull-up resistance to 5V
PA0,PB0, PB3,PB5, PB7,P00,PP0	8mA	10K	10K	
USB0DP USB1DP	4mA	1.5K	15K	
USB0DM USB1DM	4mA	180K	15K	

3.6 BT Characteristics

3.6.1 Transmitter

Basic Rate

Table 3-6

Parameter		Min	Typ	Max	Unit	Test Conditions
RF Transmit Power		-	4	6	dBm	25°C, Power Supply VBAT=3.7V 2441MHz DH5
RF Power Control Range		-	20	-	dB	
20dB Bandwidth		-	950	-	KHz	
In-band spurious Emissions (BQB Test Mode RF_Tx Power=4dBm)	F=F ₀ ±1MHz	-	-20	-	dBm	
	F=F ₀ ±2MHz	-	-45	-	dBm	2441MHz DH5
	F=F ₀ ±3MHz	-	-35	-	dBm	
	F=F ₀ ±>3MHz	-	-40	-	dBm	

Enhanced Data Rate

Table 3-7

Parameter		Min	Typ	Max	Unit	Test Conditions
Relative Power		-	-1	-	dB	25°C, Power Supply VBAT=3.7V 2441MHz 2DH5
$\pi/4$ DQPSK Modulation Accuracy	DEVM RMS	-	4	-	%	
	DEVM 99%	-	12	-	%	
	DEVM Peak	-	9	-	%	
In-band spurious Emissions (BQB Test Mode RF_Tx Power=4dBm)	F=F ₀ ±1MHz	-	-4	-	dBm	2441MHz 2DH5
	F=F ₀ ±2MHz	-	-30	-	dBm	
	F=F ₀ ±3MHz	-	-30	-	dBm	
	F=F ₀ ±>3MHz	-	-37	-	dBm	

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3.6.2 Receiver

Basic Rate

Table 3-8

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity		-	-91	-	dBm	25°C,
Co-channel Interference Rejection		-	6	-	dB	
Adjacent Channel selectivity C/I	+1MHz	-	-7	-	dB	Power Supply
	-1MHz	-	-7	-	dB	VBAT=3.7V
	+2MHz	-	-37	-	dB	2441MHz
	-2MHz	-	-39	-	dB	DH5
	+3MHz	-	-32	-	dB	
	-3MHz	-	-43	-	dB	

Enhanced Data Rate

Table 3-9

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity		-	-93	-	dBm	25°C,
Co-channel Interference Rejection		-	8	-	dB	
Adjacent Channel selectivity C/I	+1MHz	-	-14	-	dB	Power Supply
	-1MHz	-	-15	-	dB	VBAT=3.7V
	+2MHz	-	-36	-	dB	2441MHz
	-2MHz	-	-39	-	dB	2DH5
	+3MHz	-	-29	-	dB	
	-3MHz	-	-43	-	dB	

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3.6.3 BLE

1M Data Rate

Table 3-10

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity		-	-95	-	dBm	25°C Power Supply VBAT=3.7V 2440MHz
RF Transmit Power		-	6.5	8	dBm	
In-band Spurious Emission	M-N =2MHz	-	-35	-	dBm	
	M-N ≥3MHz	-	-33	-	dBm	
Modulation Characteristics	Δf1 avg	-	250	-	KHz	
	Δf2 99%	-	210	-	KHz	
	Δf1avg/Δf2avg	-	0.9	-	/	
Carrier Frequency Offset		-15	-	+15	KHz	
Frequency Drift		-25	-	+25	KHz	
Frequency Drift Rate		-5	-	+5	KHz/50us	

2M Data Rate

Table 3-11

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity		-	-92	-	dBm	25°C Power Supply VBAT=3.7V 2440MHz
RF Transmit Power		-	6.5	8	dBm	
In-band Spurious Emission	M-N =4MHz	-	-40	-	dBm	
	M-N =5MHz	-	-40	-	dBm	
	M-N ≥6MHz	-	-40	-	dBm	
Modulation Characteristics	Δf1 avg	-	500	-	KHz	
	Δf2 99%	-	430	-	KHz	
	Δf1avg/Δf2avg	-	0.9	-	/	
Carrier Frequency Offset		-20	-	+20	KHz	
Frequency Drift		-25	-	+25	KHz	
Frequency Drift Rate		-5	-	+5	KHz/50us	

Long Range

Table 3-12

Parameter	Min	Typ	Max	Unit	Test Conditions
Sensitivity LE 125K(S8)	-	-102	-	dBm	VBAT=3.7V,25°C
Sensitivity LE 500K(S2)	-	-99	-	dBm	2440MHz

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4. Package Information

4.1 QFN32(4mm*4mm)

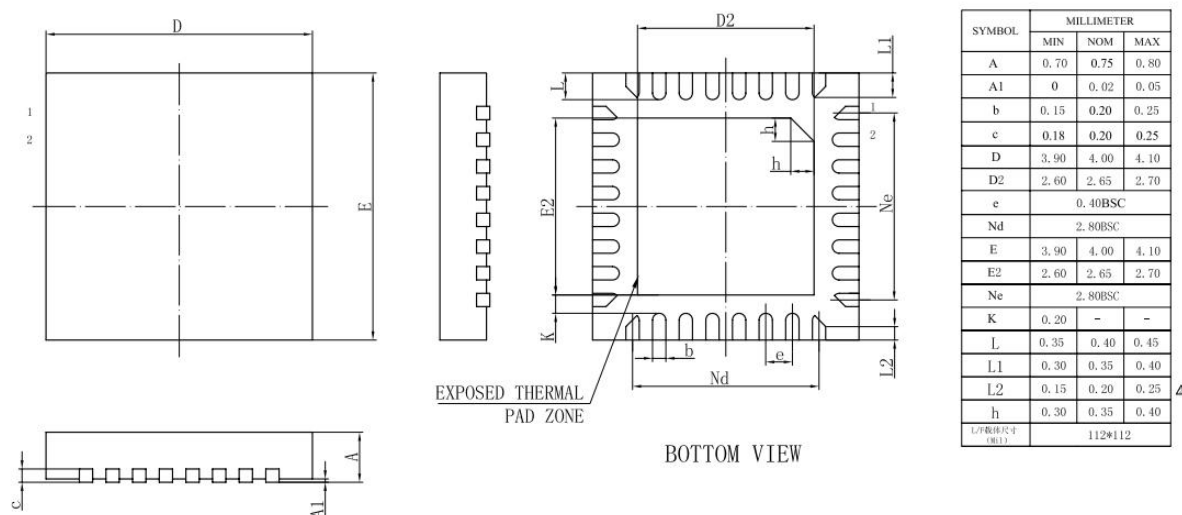
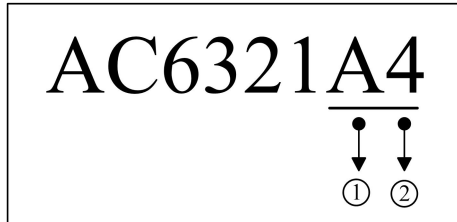


Figure 4-1 AC6321A_QFN32 Package

5. Package Type Specification



- ①Represents different packages
②Represents different memory sizes
2: 2Mbit Flash
4: 4Mbit Flash

6. Revision History

Date	Revision	Description
2021.01.22	V1.0	Initial Release
2022.07.19	V1.1	Update Bluetooth Feature
2023.11.28	V1.2	Add BLE parameter
2023.12.13	V1.3	Update Bluetooth Feature
2025.01.09	V2.0	Update Bluetooth Feature, Update Block Diagram, Add Pin Description Note